UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,294	04/22/2004	Yong-Uk Lee	YOM-0266	7218

23413 7590 08/27/2007
CANTOR COLBURN, LLP
55 GRIFFIN ROAD SOUTH
BLOOMFIELD, CT 06002

EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/829,294	LEE ET AL.
	Examiner	Art Unit
	Abbas I. Abdulselam	2629

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to a communication filed on May 24, 2007. Claims 1-12 and 14-23 are pending. Claim 13 is canceled.

Response to Arguments

2. Applicant's arguments filed on May 24, 2007 with respect to claims 14-19 have been fully considered but they are not persuasive.

3. Applicant's arguments with respect to claims 1-12 and 20-23 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claim 14, applicant argues that the cited reference Hasegawa et al. (USPN 7173602) does not teach a semiconductor layer formed on the source and the drain electrode.

However, as shown in the art rejection below, Hasegawa teaches an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501) col. 9, lines 11-14, Fig. 7 (403, 501).

With respect to claim 15, applicant argues that the cited references Hasegawa et al. (USPN 7173602) and Amundson et al. (USPN 6545291) alone or in combination do not teach "a first pixel electrode overlapping one of the gate lines and the data lines a second pixel electrode overlapping the one of gate line and the data line".

However, as shown in the art rejection below, Hesgawa teaches a pixel electrode (col. 10, lines 5-6, Fig. 8 (405)), and discloses as shown in Fig. 6, a second electrode layer 404 in the thin film piezoelectric transducer 208 is drawn parallel to the gate line 201 and is grounded, and a third electrode layer 405 of the thin film piezoelectric transducer 208 becomes the pixel

electrode of the electrophoretic ink display. Note that since a third electrode layer 405 is a pixel electrode, the second electrode layer 404 could also be a second pixel electrode as long as there is a functional equivalence.

Hasegawa does not teach, "a first pixel electrode overlapping one of the gate lines and the data lines a second pixel electrode overlapping the one of gate line and the data line".

Amundson on the other hand teaches a pixel electrode (320) having an overlap with a portion of select line (310) (col. 12, lines 25-32), and discloses the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display (col. 2, lines 54-58, Fig. 5a (330, 320)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display shown in Fig. 8 with Amundson's overlapping pixel electrode (320) as configured in Fig. 5A, because the use of overlapping pixel electrode (320) enables good use of available space under pixel electrode of electrophoretic

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al. (USPN 7173602).

Regarding claim 14, Hasegawa et al. (hereinafter = "Hasegawa") teaches an electrophoretic display comprising *(col. 6, lines 55-56, an electronic ink display)*; a substrate *(col. 9, line 14, Fig. 7 (501) an insulating substrate (501))*; and a thin film transistor formed on a surface of the substrate *(col. 9, line 9, a TFT)* this thin film transistor comprising a source electrode and a drain electrode formed on the substrate *(col. 9, lines 11-14, Fig. 7 (403, 501), an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501))*; a semiconductor layer formed on the source and the drain electrode *(col. 9, lines 9-14, Fig. 7 (401, 403), the electrode layer (403) and polycrystalline silicon layer (401), col. 9, lines 11-14, Fig. 7 (403, 501), an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501))*; an insulation layer formed on the semiconductor layer *(col. 9, lines 9-10, Fig. 7 (502, 401) a gate insulating film (502) and the polycrystalline silicon layer (401))*; and a gate electrode formed on the insulation layer *(col. 9, lines 10, Fig. 7 (502, 503), the gate insulating film (502) and gate electrode (503))*.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 20-21 and 23 are rejected under 35 U.S.C. 103(a)) as unpatentable over Amundson et al. (USPN 6545291) in view of Drzaic et al. (USPN 7030412).

Regarding claim 1, Amundson et al. (hereinafter = "Amundson") teaches an electrophoretic display *(col. 4, lines 54-55)*, comprising: a gate line which extends in a first direction *(col. 12, line 27, Fig, 5A (310), select line (310))*; a data line which extends in a second direction in a second direction substantially perpendicular to the first direction, *(col. 10, line 53, Fig. 5A (330), data line (330), as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330))*; pixel electrode overlapping the one of gate line and data line *(col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that a data line (330) and a pixel electrode (320) are configured to be one on top of the other or overlaps)*, pixel electrode overlapping

the one of gate line and the data line" (*(col. 2, lines 54-58, Fig. 5a (330, 320) the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display. Note that as shown in Fig. 5A, the pixel electrode (320) overlaps the data line (330), and a portion of the data line (330) is between the two signal lines (310)).*

Amundson does not specifically teach two pixel electrodes as a "first pixel electrode" and "second pixel electrode".

Drzaic on the other hand teaches a first pixel electrode and a second pixel electrode provided adjacent to the display medium such that the pixel electrode 94 is over the preceding gate line 53 as shown in Fig. 9 (col. 2, lines 35-37, col. 8, line 67 and col. 9, lines 1-2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) of electrophoretic display shown in Fig. 5B with Drzaic's use of two pixel electrodes, because the use of the pixel electrodes helps achieve electrophoretic display with acceptable leakage currents level as taught by Drazaic.

Regarding claim 20, Amundson teaches an electrophoretic display *(col. 4, lines 54-55)*), comprising; a gate line which extends in a first direction *(col. 12, line 27, Fig. 5 (310), select line (310));* a data line which extends in a second direction substantially perpendicular to the first direction *(col. 10, line 53, Fig. 5A (330), data line (330), as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330))*; a first pixel electrode overlapping one of the gate line and data line *(col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that a data line (330) and a pixel electrode (320) are configured to be one on top of the other or overlaps)*; a common electrode *(col. 7, lines 43-45, bounding electrodes, col. 8, lines 19-24, multiple pair of electrodes (30, 40) per capsule (20), it is inherent in the electrophoretic display that one of the bounding electrode is a common electrode)*; and a plurality of micro-capsules *(col. 8, lines 39-43, Fig. 1 (20), multiple capsules 20 may be positioned, col. 7, lines 35-38, individual electrophoretic phases may be referred as capsules or microcapsules)*, wherein each of the microcapsules of the plurality of microcapsules comprises electric ink containing a plurality of color pigment particles, *(col. 6, lines 12-19, particles may be encapsulated in the capsules, and include dyed pigments and are dispersed in a suspending fluid, and col. 7, lines 54-55, Fig. 1A (20, 25, 50), a capsule (20) contains at least one particle (50) dispersed in a suspending*

fluid (25)), wherein a color of the plurality of color pigment particles is at least one of red, green, blue, cyan, yellow, magenta black and white *(col.8, lines 5-6, particles may be colored any one of a number of colors, and col. 9, lines 31-32, blue particles)*.

Amundson does not teach "a second pixel electrode overlapping the one of gate line and the data line".

Drzaic on the other hand teaches a first pixel electrode and a second pixel electrode provided adjacent to the display medium such that the pixel electrode 94 is over the preceding gate line 53 as shown in Fig. 9 (col. 2, lines 35-37, col. 8, line 67 and col. 9, lines 1-2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) of electrophoretic display shown in Fig. 5B with Drzaic's pixel electrode 94 (which overlaps gate line 53) as configured in Fig. 9, because the use of the pixel electrode 94 helps achieve electrophoretic display with acceptable leakage currents level as taught by Drazaic.

Regarding claims 2, 21 and 23, Amundson teaches a portion of the first pixel electrode overlaps a portion of a width of the data line extending in the second direction/first direction between adjacent gate lines the data line *(col. 2, lines 54-58, Fig. 5a (330, 320) the*

pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display. Note that as shown in Fig. 5A, the pixel electrode (320) overlaps the data line (330), and a portion of the data line (330) is between the two signal lines (310)).

8. Claims 7 and 11are rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Amundson et al. (USPN 6545291).

Regarding claim 7, Drzaic (USPN 6518949) teaches an electrophoretic display *(col. 1, line 59-61, col. 1, line 67 and col. 2, lines 1-2 and Fig. (8*)) comprising; a substrate *(Fig. 8(92'), substrate 92')*; a gate line which extends in a first direction *(Fig. 7 (106), row electrode 106)*; a data line which extends in a second direction substantially perpendicular to the first direction *(Fig. 7 (104), a column electrode 104, as shown in Fig. 7, the column electrode 104 is perpendicular to the row electrode 106)*; a thin film transistor comprising a channel *(Fig. 7 (100), transistor (100), Fig. 8 (90'), transistor (90'))*; a gate electrode *(col. 10, lines 9, Fig. 8 (96'), gate electrode (96'))*, a source electrode *(col. 10, lines 7, Fig. 8(98'), source electrode (98'))*; a drain electrode a semiconductor layer *(col. 10, line 8, col. 10, lines 4, Fig. 8(99', 97'), a drain electrode 99'and a semiconductor layer 97')*; and an opaque layer *(col. 10, line 6, Fig. 8(110) a barrier layer (110), and col. 9, lines 50-51, a barrier layer is opaque)*, wherein the opaque layer formed on the semiconductor

layer and disposed over the channel of the thin film transistor*(col. 10, lines 3-4, the barrier layer (110) is positioned over at least a semiconductor layer (97'), and Fig. 8 (96', 110, 97'), Fig. 8 shows the semiconductor layer 97'is between the gate electrode, 96'and the barrier layer (110));*

While , Drzaic (USPN 6518949) teaches providing a plurality of pixel electrodes adjacent the second surface of the display media (col. 2, lines 17-20),

Drzaic does not specifically teach a first pixel electrode overlapping one of the gate line and the data line; and a second pixel electrode overlapping the one of the gate line and the data line.

Amundson on the other hand teaches a pixel electrode (320) having an overlap with a portion of select line (310) as shown in Fig. 5A. Amundson also teaches the pixel electrode and the data line electrode is interdigitated such that the data line electrode comprises a data line of the display (see Fig. 5A (310, 330), col. 2, lines 55-58 , col. 12, lines 25-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic's electronic display shown in Fig. 7 with Amundson's overlapping pixel electrode (320) as configured in Fig. 5A, because the use of overlapping pixel electrode (320)

enables good use of available space under pixel electrode of electrophoretic display as taught t by Amundson (col. 12,lines 17-20).

Regarding claim 11, Drzaic teaches wherein the first pixel electrode is made of opaque material *(col. 2, lines 38-41, a substrate that can be opaque, and col. 8, lines 15-17, a substrate that can be patterned to serve as the pixel electrode)*, and wherein the first pixel electrode and the second overlap the channel of the thin film transistor *(col. 4, lines 23-25, Fig. 1a (20) the transistors 20 are located underneath the pixel electrodes (18))*.

9. Claims 3, 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Drzaic et al. (USPN 7030412) further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 3, 6 and 22, while Amundson as modified by Drzaic teaches an insulating layer is/interposed/formed between the data line and one of the first pixel electrode and the second pixel electrode*(col. 11, lines 17-20, an insulating layer (170) separating a drain electrode (130) from the pixel electrode (320), and col. 10, lines 52-53, Fig. 3 (130, 330), the drain electrode (130) of TFT is connected to a data line 330)*,

Amundson modified by Drzaic does not teach the insulating layer having a dielectric constant lower than 4, with the insulating layer being made of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64 and col. 13, lines 48-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Amundson's (as modified by Drzaic) insulating layer (170) of an electrophoretic display shown in Fig. 5B with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 16-18 and col. 13, lines 59-60).

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Izumi et al. (USPN 7148867).

Regarding claim 4, *while Amundson teaches various materials may be used to create electrophoretic displays, and cites as exemplary particles including titania, which may be coated in one or two layers in a metal oxide (col. 6, lines 52-54 and col. 6, lines 61-63),*

Amundson does not teach "the data line is made of a metal selected from agroup consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Note that even though Amundson teaches electrophoretic display and Izumi teaches liquid crystal display, the functionality of Amundson's data line (330) and Izmui's source line (25) is the same for both type of displays.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Amundson's data line (330) of an electrophoretic display shown in Fig. 5A with Izumi's Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10-13).

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Drzaic et al. (USPN 7030412).

Regarding claim 5, Amundson teaches a thin film transistor comprising a channel *(col. 11, lines 36-37, Fig. 4B, a TFT with a channel);* a source electrode *(col. 11, lines 6-7, Fig. 5A(120), a source electrode (120));* a drain electrode *(col. 11, lines 6-7, Fig. 5A (130), a drain electrode (130));* and wherein the first pixel electrode and the second pixel electrode overlaps the channel of the thin film transistor *(col. 11, lines 45-47, a TFT channel is substantially under the pixel electrode),*

While Amundson teaches electrodes (30, 40) that could be fabricated from opaque materials (col. 8, lines 55-56),

Amundson does not teach the first pixel electrode and the second pixel electrode are made of opaque material.

Drzaic et al. (USPN 7030412) on the other hand teaches a pixel electrode (104) as shown in Fig. 10 that can be transparent or opaque (col. 10, lines 61-62 and Fig. 10 (104)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) of an electrophoretic display shown in Fig. 5A with Drzaic's opaque characteristics of the pixel electrode (104), because the use of an opaque

pixel electrode helps function an electronic display 100 by being boned to a display medium as taught by Drzaic (col. 8, lines 52-56).

12. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Amundson et al. (USPN 6545291) and further in view of Hirota (USPN 7098980).

Regarding claim 8, While Drzaic as modified by Amundson teaches a data line *(col. 8, line 56, Fig. 7 (104), a column electrode (104)); and a gate line (col. 8, line 57, Fig. 7 (106), a row electrode (106))*;

Drzaic does not teach " the inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees".

Hirota (USPN 7098980) on the other hand teaches as a scanning line (1), a pixel electrodes 5 and a common electrodes 6 are so configured as to be bent relative to the alignment direction of N-type liquid crystal. Hirota further teaches that the bent angle 10 can be selected to be an angle with the best display performance as long as the angle is within the range from 60 degrees to 120 degrees except 90 degrees (col. 5, lines 28-34, Fig. 5 (1, 5, 6)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic's (as modified by Amundson) row electrode (106) of an electronic display shown in Fig. 7 with Hirota's bendable electrode having a range of bending angle (60-120 degrees, (90) excepted), which includes a range of 60-80 degrees, because the use of bendable electrode or line makes it possible to achieve a large screen, wide visual angle display with high yield and low cost as taught by Hirota (col. 5, lines 65-67).

13. Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Amundson et al. (USPN 6545291), and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 9 and 12, while Drzaic as modified by Amundson teaches an insulating layer formed between the data line and one of the first pixel electrode and the second pixel electrode *(col. 4, lines 61-65, Fig. 1 C (18', 21, 15'), a pixel electrode (18') and a column electrode 15' and insulator (21) are configured)*,

Drzaic does not teach the insulating layer having a dielectric constant smaller than 4 with the insulating layer being made of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide

containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Drzaic's (as modified by Amundson) insulator (21) of an electronic display shown in Fig. 1c with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

14. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Amundson et al. (USPN 6545291) and further in view of Izumi et al. (USPN 7148867).

Regarding claim 10, *while Drzaic as modified by Amundson teaches formation of column electrodes through conductive coatings, which may be Indium, Tin Oxide (ITO) or some other suitable conductive material (col. 11, lines 10-13, col. 11, lines 19-20),*

Drzaic as modified by Amundson does not specifically teach "the data line is made of metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) that may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic' s (as modified by Amundson) column electrode (104) of an electronic display shown in Fig. 7 with Izumi's use of Tantalum (Ta)-patterned metal film for source lines, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of a display device (100) as taught by Izumi.

15. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Amundson et al. (USPN 6545291).

Regarding claim 15, while Hasegawa teaches a gate line which extends in a first direction *(col. 10, lines 1-2, Fig. 8 (201) a gate line)*; a data line which extends in a second

direction substantially parallel to the first direction *(col. 10, lines 1-2, Fig. 8 (203), data line (203)),*

Hesgawa teaches a pixel electrode (col. 10, lines 5-6, Fig. 8 (405)), and discloses as shown in Fig. 6, a second electrode layer 404 in the thin film piezoelectric transducer 208 is drawn parallel to the gate line 201 and is grounded, and a third electrode layer 405 of the thin film piezoelectric transducer 208 becomes the pixel electrode of the electrophoretic ink display. Note that since a third electrode layer 405 is a pixel electrode, the second electrode layer 404 could also be a second pixel electrode as long as there is a functional equivalence.

Hasegawa does not teach, "a first pixel electrode overlapping one of the gate lines and the data lines a second pixel electrode overlapping the one of gate line and the data line".

Amundson on the other hand teaches a pixel electrode (320) having an overlap with a portion of select line (310) (col. 12, lines 25-32), and discloses the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display (col. 2, lines 54-58, Fig. 5a (330, 320)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display shown in Fig. 8 with Amundson's overlapping pixel electrode (320) as

configured in Fig. 5A, because the use of overlapping pixel electrode (320) enables good use of available space under pixel electrode of electrophoretic display as taught t by Amundson (col. 12,lines 17-20).

16. Claim 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Amundson et al. (USPN 6545291) and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 16 and 19, While Hasegawa teaches an insulating layer is formed between the data line and one of the first pixel electrode and the second pixel electrode, (*col. 9, lines 10-11, col. 9, lines 15-16, col. 10, lines 5-6, Fig. 7 (403, 502, 504, 405), an electrode layer (403), interlayer insulating film (504) & gate insulating film (502), and pixel electrode (405)),*

Hasegawa as modified by Amundson does not teach the insulating layer has a dielectric constant smaller than 4.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Amundson) insulating films (502, 504) of an electrophoretic display shown in Fig. 7 with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

17. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Amundson et al. (USPN 6545291) and further in view of Izumi et al (USPN 7148867).

Regarding claim 17, *while Hasegawa teaches electrode layers including a layer of titanium (col. 3, lines 53-55),*

Hasegawa as modified by Amundson does not specifically teach "the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti".

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Amundson) data line (203) of an electrophoretic display shown in Fig. 8 with Izumi's Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10-13).

18. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Amundson et al. (USPN 6545291) and further in view of Hirota (USPN 7098980).

Regarding claim 18, Hasegawa as modified by Amundson does not teach " the inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees".

Hirota (USPN 7098980) on the other hand teaches as a scanning line (1), pixel electrodes 5 and a common electrode 6 are so configured as to be bent relative to the alignment direction of N-type liquid crystal. Hirota further teaches that the bent angle 10 can be selected to be an angle with the best display performance as long as the angle is within the range from

60 degrees to 120 degrees except 90 degrees (col. 5, lines 28-34, Fig. 5 (1, 5, 6)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Amundson) gate lines (201) of a display shown in Fig. 8 with Hirota's bendable electrode having a range of bending angle (60-120 degrees, (90) excepted), which includes a range of 60-80 degrees, because the use of bendable electrode or line makes it possible to achieve a large screen, wide visual angle display with high yield and low cost as taught by Hirota (col. 5, lines 65-67).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas Abdulselam

Examiner

Art Unit 2629

August 18, 2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600